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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,184	03/29/2004	William Radke	500988.02 (30064/US/2)	5824
7590	02/03/2005		EXAMINER	
Kimton N. Eng, Esq. DORSEY & WHITNEY LLP Suite 3400 1420 Fifth Avenue Seattle, WA 98101			CHAUHAN, ULKA J	
			ART UNIT	PAPER NUMBER
			2676	
DATE MAILED: 02/03/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	RADKE ET AL.	
10/813,184	Examiner	Art Unit
	Ulka J. Chauhan	2676

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 18 October 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 31-49 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 31-49 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

1. Claims 1-31 are cancelled; claims 32-49 are newly added and pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 45-49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 45 recites the limitation “the first memory” in line 12, and the limitation “the output bus” in line 24. There is insufficient antecedent basis for these limitations in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 32, 33, 34, and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,987,628 to Von Bokern et al.**

7. As per claims 32, 34, and 38, Von Bokern teaches correcting corrupted data in a memory subsystem in which a subsystem controller 12 comprises a memory correction logic 35, error reporting logic 43, eic logic 39, and read-merge-write logic 41 [Fig. 2]. Von Bokern discloses that data values and ECC values output from the memory subsystem 14 are supplied to the ECC logic 39 (*reading data and an associated error correction code from a location in the memory*

array) [col. 5 lines 45-47 and Fig. 2]. For each data value received from the memory subsystem 14, the ECC logic 39 determines whether the data value is corrupted, attempts to recover the data value, and then forwards the data value to the RMW logic 41 or to various read buffers (not shown) associated with respective requesting agents (storing the data in a memory) [col. 5 lines 47-57]. The RMW logic 41 having a RMW buffer 105, buffers the corrected data and writes the data to the memory subsystem 14 at an address provided by the memory correction logic 35 via the ECC generator 97 and ECC logic 39 such that, data read from memory may be merged with data from other write buffers and written back to memory along with its corresponding ECC (modifying at least a portion of the data; and when writing the modified data to the memory array, updating the data stored in the memory with the modified portion of the data; calculating a new error correction code based on the updated data in the memory; and storing the updated data and the new error correction code to the location in the memory array) [col. 5 line 61-col. 6 line 4, col. 13 lines 57-65, and col. 14 lines 3-20].

8. As per claim 33, APA discloses that graphics processing operations include a read-modify-write (RMW) operation comprising the steps of reading data that will be processed from the embedded memory, modifying the retrieved data during processing, and writing the modified data back to the embedded memory [0003]. Von Bokern discloses that the RMW logic 41 having a RMW buffer 105, buffers the corrected data and writes the data to the memory subsystem 14 at an address provided by the memory correction logic 35 via the ECC generator 97 and ECC logic 39 such that, data read from memory is merged with data from other write buffers and written back to memory along with its corresponding ECC [col. 5 line 61-col. 6 line 4, col. 13 lines 57-65, and col. 14 lines 3-20].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. **Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,987,628 to Von Bokern et al, and U.S. Patent No. 5,809,228 to Langendorf et al, and U.S. Patent No. 6,151,658 to Magro.**

12. As per claim 35, Von Bokern discloses that the RMW buffer 105 writes the corrected data to the memory subsystem 14 at an address provided by the memory correction logic 35 [col. 5 line 61-col. 6 line 4, col. 13 lines 57-65, and col. 14 lines 3-20]. Von Bokern does not expressly teach *determining whether a write address corresponds to an address of data previously stored in the memory; accessing the data stored in the memory based on the write address if correspondence is determined; and logically combining the stored data and the modified data together and storing the modified data in the memory location in the memory*

where the data was previously stored. Magro teaches a write buffer FIFO architecture that includes a write buffer controller and RAM containing a CAM address store and a RAM data store [Fig. 2]. The CAM compares an input write address to the addresses present in the CAM address store to detect an address hit which signals the data store to store the input write data at the address detected by the CAM [Abstract]. The CAM also detects whether an input read address provided to a memory device is related to an address in the address store, the read data at the related address in the address store is retrieved and merged with the read data from the memory device to produce valid read data, thus enhancing the general FIFO function with write merging, write collapsing, and read merging [Abstract]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Von Bokern and Magro such that the RMW buffer of Von Bokern's invention is implemented with the write buffer FIFO architecture taught by Magro in order to enhance the function of Von Bokern's RMW buffer with write merging, write collapsing, and read merging taught by Magro.

13. Claims 36, 39-41, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,987,628 to Von Bokern et al and U.S. Patent No. 6,041,168 to Williams et al.

14. As per claim 36, Von Bokern does not expressly teach *substantially concurrent with the reading and storing of data, updating second data previously stored in a second memory with a modified portion of the second data; and substantially concurrent with the updating of the data, reading third data and storing the third data in the second memory.* Williams teaches improvements in the construction and operation of a data FIFO between buffer manager and a storage device. Williams discloses that an ECC circuit 34 is provided to perform known error

correction and control functions on data read from a storage 26, where the ECC circuit 34 interfaces to a FIFO 30 comprising three FIFO sections 40-43, enabling faster RMW cycles in the correction of the data contained in the FIFO 30 [col. 4 lines 44-59]. A first data is read from storage and written to FIFO 40; a second data is read from storage and written to FIFO 41 concurrently with operating the ECC circuit to correct the data in FIFO 40 and writing the corrected data back to FIFO 40; and a third data is read from storage and written to FIFO 42 concurrently with operating the ECC circuit to correct the data in FIFO 41 and writing the corrected data back to FIFO 41 [col. 5 lines 7-53]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Von Bokern and Williams whereby the RMW logic 41 including the RMW buffer of Von Bokern's invention is implemented to include two of the FIFOs operating in the pipelined manner taught by Williams in order to enable faster RMW cycles in the correction of data read from a memory.

15. Claims 39-41, and 44 are similar in scope to claims 33, 34, 36, and 38, and are rejected under the same rationale.

16. **Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,987,628 to Von Bokern et al and Applicant's Admitted Prior Art (APA) in paragraphs [0002] to [0008] of the specification.**

17. As per claim 37, Von Bokern does not expressly teach correcting corrupted data in an embedded memory. APA discloses that graphics processing systems often include embedded memory to increase the throughput of processed graphics data, such that the processing elements of the graphics processing system retrieve, process, and provide graphics data quickly and

efficiently, increasing the processing throughput [0002]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Von Bokern and APA such that the graphics subsystem 16 of Von Bokern's invention is implemented to include an embedded memory as disclosed by APA and the method of correcting corrupted data in a memory subsystem is applied to this embedded memory in order to provide data integrity as well as increased throughput for the graphics subsystem.

18. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,987,628 to Von Bokern et al, U.S. Patent No. 6,041,168 to Williams et al, and U.S. Patent No. 6,151,658 to Magro.

19. As per claim 42, Von Bokern discloses that the RMW buffer 105 writes the corrected data to the memory subsystem 14 at an address provided by the memory correction logic 35 [col. 5 line 61-col. 6 line 4, col. 13 lines 57-65, and col. 14 lines 3-20]. Von Bokern does not expressly teach *determining whether a write address corresponds to an address of data previously stored in the memory; accessing the data stored in the memory based on the write address if correspondence is determined; and logically combining the stored data and the modified data together and storing the modified data in the memory location in the memory where the data was previously stored*. Magro teaches a write buffer FIFO architecture that includes a write buffer controller and RAM containing a CAM address store and a RAM data store [Fig. 2]. The CAM compares an input write address to the addresses present in the CAM address store to detect an address hit which signals the data store to store the input write data at the address detected by the CAM [Abstract]. The CAM also detects whether an input read address provided to a memory device is related to an address in the address store, the read data at

the related address in the address store is retrieved and merged with the read data from the memory device to produce valid read data, thus enhancing the general FIFO function with write merging, write collapsing, and read merging [Abstract]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Von Bokern, Williams, and Magro such that the RMW buffer of Von Bokern's invention is implemented with the write buffer FIFO architecture taught by Magro in order to enhance the function of Von Bokern's RMW buffer with write merging, write collapsing, and read merging taught by Magro.

20. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,987,628 to Von Bokern et al, U.S. Patent No. 6,041,168 to Williams et al, and Applicant's Admitted Prior Art (APA) in paragraphs [0002] to [0008] of the specification.

21. As per claim 43, Von Bokern does not expressly teach correcting corrupted data in an embedded memory. APA discloses that graphics processing systems often include embedded memory to increase the throughput of processed graphics data, such that the processing elements of the graphics processing system retrieve, process, and provide graphics data quickly and efficiently, increasing the processing throughput [0002]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Von Bokern, Williams, and APA such that the graphics subsystem 16 of Von Bokern's invention is implemented to include an embedded memory as disclosed by APA and the method of correcting corrupted data in a memory subsystem is applied to this embedded memory in order to provide data integrity as well as increased throughput for the graphics subsystem.

Allowable Subject Matter

22. Claim 45 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.
23. Claims 46-49 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

24. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. US006279135B1 U.S. Patent No. US006167551A

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is (703) 305-9651. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.
26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on (703) 308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ulka J. Chauhan

Ulka J. Chauhan
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